CBCS SCHEME

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15CS34

Third Semester B.E. Degree Examination, Jan./Feb. 2023
Computer Organization

Time: 3 hrs. Max. Marks: 80

Note: Answer any FIVE full questions, choosing ONE full question from each module.

Module-1

1 a. Explain the connections between the processor and the memory with the help of block diagram. **(06 Marks)**

b. How performance of a computer can be improved by introducing Cache memory with diagram? Also explain factors affecting performance of computer. **(06 Marks)**

c. With a neat diagram, explain a single bus structure used to interconnect the functional units. **(04 Marks)**

OR

2 a. Explain Big-Endian and Little-Endian Assignments with neat diagram. **(08 Marks)**

b. Explain Basic Instruction types and different types of their representations. **(08 Marks)**

Module-2

3 a. What is an Interrupt? Explain the following methods of handling interrupts from multiple devices.
(i) Interrupt Nesting / Priority.
(ii) Daisy chain method. **(08 Marks)**

b. With neat diagram, explain how to interface printer to processor. **(08 Marks)**

OR

4 a. Explain DMA (Direct Memory Access) along with the various Registers and controllers. **(08 Marks)**

b. Elaborate Bus Arbitration methods with neat diagram. **(08 Marks)**

Module-3

5 a. With a neat diagram, explain internal organization of memory chip (2m×8 Dynamic Memory Chip). **(08 Marks)**

b. Briefly explain Direct and Associative Mapping used in Cache memory. **(08 Marks)**

OR

6 a. Discuss the concept of fast page mode. **(04 Marks)**

b. Define the following with respect to cache memory :
(i) Valid bit
(ii) Dirty bit
(iii) Flush the cache
(iv) Cache hit **(04 Marks)**

c. What is virtual memory? With a neat diagram, explain how virtual memory address is translated. **(08 Marks)**

Module-4

7 a. With a neat diagram, explain a 4-bit carry-look ahead adder along with generation and propagation functions. **(08 Marks)**

b. Using Booth Algorithm Multiply (+13) and (−6). Repeat the same with Bit-pair recoding technique. **(08 Marks)**

OR

8 a. Explain with a neat diagram, the circuit arrangement for non-restoring division process. Perform 8 ÷ 3 using the same. **(10 Marks)**

b. Explain the various IEEE standard floating point formats. **(06 Marks)**

Module-5

9 a. Explain with a neat diagram, the single Bus Organization of the Data Path inside a processor. **(08 Marks)**

b. Give the actions and control sequences for execution of instruction ADD (R3), R1. **(08 Marks)**

OR

10 a. Explain the block diagram of an embedded processor. **(08 Marks)**

b. Explain the possible ways of implementing a multiprocessor system. **(08 Marks)**

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